REMARKS

This Amendment is submitted in answer to the Office Action dated December 19, 2005.

I. REJECTION UNDER 35 U.S.C. § 112

On page 2 of the present Office Action, Claims 1, 5-6, 9 and 12-13 are rejected under 35 U.S.C. § 112, second paragraph, as indefinite based upon the recitation of certain claim features in the format permitted by 35 U.S.C. § 112, sixth paragraph. In response, Applicant has amended Claims 1, 5-6, 9 and 12-13 to eliminate the "means for" language permitted by 35 U.S.C. § 112, second paragraph, rendering moot the rejection under 35 U.S.C. § 112, second paragraph.

II. REJECTION UNDER 35 U.S.C. § 102

On page 3 of the present Office Action, Claims 1-18 are rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,697,919 to *Gharachorloo et al.* (*Gharachorloo*). That rejection is respectfully traversed, and favorable reconsideration of the claims is requested.

A. *Gharachorloo* does not disclose the "memory speculation mechanism" of exemplary independent Claim 1

Gharachorloo does not render exemplary Claim 1 unpatentable under 35 U.S.C. § 102 because that reference does not disclose a memory controller having a "memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing the system memory." At page 4 of the Office Action, *Gharachorloo's* directory 180 is cited as teaching the claimed memory speculation mechanism. However, *Gharachorloo's* directory 180 does not "store[ ] historical information regarding whether prior memory accesses were serviced by accessing the system memory" as claimed. Instead, directory 180 indicates where in the system copies of particular memory lines are cached, as shown in the table set forth in *Gharachorloo's* Figure 4. Because *Gharachorloo* does not disclose a memory controller having a memory speculation mechanism as claimed, Applicant respectfully submits that the rejection of exemplary Claim 1, similar Claims 9 and 14, and their respective dependent claims under 35 U.S.C. § 102 is overcome.

B. *Gharachorloo* does not disclose a memory controller that speculatively initiates access to system memory as recited in exemplary independent Claim 1

Gharachorloo does not render exemplary Claim 1 unpatentable under 35 U.S.C. § 102 because that reference does not disclose the following feature of Claim 1:

> ... said memory controller, responsive to a memory access request, speculatively initiates access to the system memory based upon said historical information in said memory speculation mechanism in advance of receipt of a coherency message indicating that said memory access request is to be serviced by reference to said system memory.

At pages 4-5 of the present Office Action, *Gharachorloo's* memory controller 118 is cited as disclosing the claimed memory controller. However, the Office Action then relies upon various additional passages of *Gharachorloo* as teaching the maintenance of coherency by home protocol engine 122 and remote protocol engine 124. In response, Applicant respectfully points out that none of the functions relied upon by the Examiner is performed by *Gharachorloo's* memory controller 118 or discloses memory controller 118 speculatively initiating access to *Gharachorloo's* memory subsystem 123 (which is relied upon by the Examiner as disclosing the claimed system memory). Because *Gharachorloo* does not disclose a memory controller as recited in exemplary Claim 1, Applicant respectfully submits that the rejection of exemplary Claim 1, similar Claims 9 and 14, and their respective dependent claims under 35 U.S.C. § 102 is overcome.

C. *Gharachorloo* does not disclose the features recited in exemplary dependent Claim 3

Gharachorloo also does not render exemplary Claim 3 unpatentable under 35 U.S.C. § 102 because that reference does not disclose the following features of Claim 3:

> ... said memory speculation mechanism comprises a memory speculation table that stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

At pages 5-6 of the present Office Action, the Examiner relies upon *Gharachorloo's* disclosure of instruction-level parallelism, simultaneous multithreading (SMT), and out-of-order

execution as teaching the features of Claim 3. Applicant respectfully traverses the Examiner's position because none of these features of *Gharachorloo's* processor cores discloses a memory speculation table of a memory controller that stores a per-thread history, as required by the recitation that the "memory speculation table stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores." Because *Gharachorloo* does not disclose the features recited in exemplary Claim 3, Applicant respectfully submits that the rejection of exemplary Claim 3 and similar Claims 10 and 15 under 35 U.S.C. § 102 is overcome.

D. *Gharachorloo* does not disclose the features recited in exemplary dependent Claim 4

Gharachorloo also does not render exemplary Claim 4 unpatentable under 35 U.S.C. § 102 because that reference does not disclose the following features of Claim 4:

> ... said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

At page 6 of the present Office Action, the Examiner relies, *inter alia*, upon *Gharachorloo's* disclosure of memory banks as teaching the features of Claim 4. Applicant respectfully traverses the Examiner's position because *Gharachorloo's* disclosure of memory banks does not disclose a memory speculation table of a memory controller that stores a per-bank history, as required by Claim 4. Because *Gharachorloo* does not disclose the features recited in exemplary Claim 4, Applicant respectfully submits that the rejection of exemplary Claim 4 and similar Claims 11 and 16 under 35 U.S.C. § 102 is overcome.

E. *Gharachorloo* does not disclose the features recited in exemplary dependent Claim 5

Gharachorloo also does not render exemplary Claim 5 unpatentable under 35 U.S.C. § 102 because that reference does not disclose the following features of Claim 5:

> ... wherein said memory controller speculatively initiates access in advance of a combined response for said memory access request.

At page 7 of the present Office Action, the Examiner relies upon *Gharachorloo's* column 7 as disclosing a memory controller speculatively initiating access to system memory and further relies

upon col. 11, line 19 as teaching that the access is made prior to receipt of the combined response. Applicant respectfully traverses the Examiner's position because *Gharachorloo's* column 7 nowhere discloses a memory controller, such as *Gharachorloo's* memory controller 118, speculatively initiating access to system memory. Further, col. 11, line 19 merely discloses the execution of instructions from a microcode array "to advance memory transactions," but completely fails to disclose the initiation of speculative access to system memory in advance of a combined response for the memory access request, as recited by Claim 5. Because *Gharachorloo* does not disclose the features recited in exemplary Claim 5, Applicant respectfully submits that the rejection of exemplary Claim 5 and similar Claim 17 under 35 U.S.C. § 102 is overcome.

F. *Gharachorloo* does not disclose the features recited in exemplary dependent Claim 6

Gharachorloo also does not render exemplary Claim 6 unpatentable under 35 U.S.C. § 102 because that reference does not disclose the following features of Claim 6:

> ... said memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller.

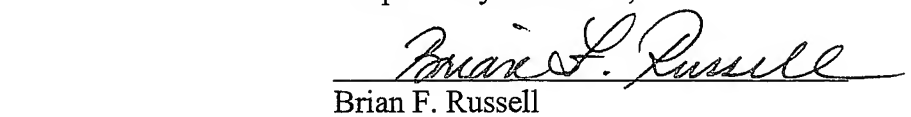
At page 8 of the present Office Action, the Examiner relies upon *Gharachorloo's* column 21, lines 59-63 as disclosing that *Gharachorloo's* cache coherence protocol enables sharing of memory lines across multiple nodes. Applicant respectfully traverses the Examiner's position because *Gharachorloo's* disclosure of a coherency protocol fails to disclose the speculative initiation of access to a system memory by a first system memory controller based upon historical information recorded by a second memory controller, as recited by Claim 6. Because *Gharachorloo* does not disclose the features recited in exemplary Claim 6, Applicant respectfully submits that the rejection of exemplary Claim 6 and similar Claims 13 and 18 under 35 U.S.C. § 102 is overcome.

III. CONCLUSION

Having now addressed and overcome each outstanding rejection, Applicant respectfully submits that all claims now pending are in condition for allowance and respectfully requests such allowance.

Please charge any fee necessary to further the prosecution of this application to IBM Corporation Deposit Account No. **09-0447**.

Respectfully submitted,



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